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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,852	10/22/2001	Ko-Yan Shih	JCLA7022	9319

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J.C. PATENTS, INC.
SUITE 250
4 VENTURE
IRVINE, CA 92618

EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/039,852

Applicant(s)

SHIH ET AL.

Examiner

John P Trimmings

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the Applicant's amendment dated 11/12/2004.

Claims 1, 2, 5, 6, 8 and 10 were amended by the applicant.

Claims 1-11 are pending in this Office Action.

Response to Amendment

1. In view of the changes to the Specification, the examiner withdraws all objections to the Specification, and approves said changes.
2. In view of the changes to Figure 4, the examiner withdraws all objections to the drawing, and approves said changes.
3. In view of the amendments to Claims 2, 6 and 8, the examiner withdraws the rejections of said claims under 35 USC 112 second paragraph.
4. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new grounds of rejection. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 102

5. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al., U.S. Patent No. 5592493.

As per Claim 1:

Crouch et al. teaches a method of testing a chip that comprises an intellectual product circuit module (see Title and column 5 line23), the method comprising: providing a test pattern (column 9 lines 10-14); sequentially configuring a plurality of registers in a plurality of different states according to the test pattern (for example FIG.2 70-84 and column 6 lines 1-5); and after all of the registers are configured with the test pattern (column 6 lines 10-11), providing a test activating signal to the intellectual product circuit module (column 6 lines 11-22) in a next state (column 6 lines 11-22 ; "next rising edge of the clock"), so that the intellectual product circuit module operates according to the test pattern from the registers (column 6 lines 1-29).

As per Claim 2:

Crouch et al. teaches a circuit for testing a chip (see Abstract) that comprises an intellectual product circuit module (FIG.1 12, 14, 16, 18, 20, 22), the circuit for testing the chip comprising: a plurality of registers (for example: FIG.2 70-84), coupled to the intellectual product circuit module (for example FIG.2 66) to output signals stored in the registers to the intellectual product circuit module (FIG.2 66); and a multiplexing finite state machine controller (FIG.2 10), coupled to the intellectual product circuit module and the registers (see FIG.1), wherein the multiplexing finite state machine controller receives a test pattern (column 6 lines 1-9) and sequentially configures the registers with the test pattern in a plurality of different states (column 9 lines 10-14), after all of the registers are configured with the test pattern (column 6 lines 10-11), in a next state (column 6 lines 11-22 ; "next rising edge of the clock") the multiplexing finite state machine controller further provides a test activating signal to the intellectual product

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circuit module (column 6 lines 9-22) so that the intellectual product circuit module is operated and tested according to outputs of the registers (example: column 6 lines 1-30).

As per Claim 3:

Crouch et al. teaches the circuit according to claim 2, wherein the intellectual product circuit module further comprises a plurality of ports coupled to the registers (example: FIG.2. 64, 77 and 76 to 66).

As per Claim 4:

Crouch et al. teaches the circuit according to claim 2, wherein the test activating signal includes a synchronous clock signal (FIG.1 PCLK and column 6 line 25).

As per Claim 5:

Crouch et al. teaches the circuit according to claim 2, wherein each of the registers further comprises an enable input terminal (FIG.1 MTM, TSTADDR, S_SE, STD1) coupled to the multiplexing finite state controller capable of controlling the registers and asserting an enable signal to enable the registers to buffer the test pattern (column 7 lines 54-67 and column 8 lines 1-26).

As per Claim 6:

Crouch et al. teaches a circuit for testing a chip that comprises a plurality of intellectual product circuit modules (FIG.1 12, 14, 16, 18, 20, 22), comprising: a multiplexer controller (FIG.2 46), coupled to the intellectual product circuit modules (FIG.2 50 and 24) to selectively output a test result from the intellectual product circuit

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modules (FIG.2 54 or SDO 58 as per column 10 lines 7-17); a plurality of registers (for example: FIG.2 70-84), coupled to the intellectual product circuit modules to output signals stored in the registers to the intellectual product circuit modules (FIG.2 66); and a multiplexing finite state machine controller (FIG.2 10), coupled to the intellectual product circuit modules (FIG.2 66), the multiplexer controller and the registers (see FIG.1), the multiplexing finite state machine controller receiving a test pattern (column 6 lines 1-9) to sequentially configure the registers with the test pattern in a plurality of different states (column 9 lines 10-14), and after all of the registers are configured with the test pattern (column 6 lines 10-11), providing a test activating signal to one of the intellectual product circuit modules (column 6 lines 9-22) in a next state (column 6 lines 11-22 ; "next rising edge of the clock"), so that the intellectual product circuit module is operated according to the output of the registers (example: column 6 lines 1-30), and the multiplexing finite state machine controller further controlling a multiplexer controller (FIG.2 10 MUX) to selectively output the test results (FIG.2 SCAN DATA OUT).

As per Claim 7:

Crouch et al. further teaches the circuit according to claim 6, wherein each of the intellectual product circuit modules comprises a plurality of ports coupled to the registers (example: FIG.2. 64, 77 and 76 to 66).

As per Claim 8:

Crouch et al. further teaches the circuit according to claim 6, wherein the multiplexer controller further comprises a select input terminal coupled to the multiplexing finite state machine controller (FIG.1 TSTADDR), so that the multiplexing

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finite state machine controller controls the multiplexer controller to selectively output the test result (FIG.2 10 and SCAN DATA OUT).

As per Claim 9:

Crouch et al. further teaches the circuit according to claim 6, wherein the test-activating signal comprises a synchronous clock signal (FIG.1 PCLK and column 6 line 25).

As per Claim 10:

Crouch et al. further teaches the circuit according to claim 6, wherein each of the registers further comprises an enable input terminal (FIG.1 MTM, TSTADDR, S_SE, STDI) coupled to the multiplexing finite state machine controller, which respectively controls and enables the registers to buffer the test pattern (column 7 lines 54-67 and column 8 lines 1-26).

As per Claim 11:

Crouch et al. further teaches the circuit according to claim 6, wherein the chip is a system on chip (column 1 lines 5-30).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (703) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

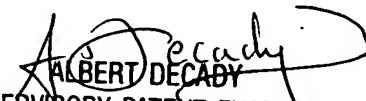
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